

REMARKS/ARGUMENTS

Claims 1-8 are pending. Claim 1 has been amended to correct minor informalities. No new matter has been introduced. Applicant believes the claims comply with 35 U.S.C. § 112.

Section 112 Rejection

The Examiner rejects claims 1-8 under 35 U.S.C. § 112, second paragraph, on the ground that "a portion of a first selected one of said stacked metal layers and a portion of a second selected one of said stacked metal layers, said second selected stacked metal layer portion above and adjacent said first selected stacked metal layer portion" is unclear.

The specific embodiment as shown in Figs. 4A and 4B is used to illustrate the elements of the claim 1, but it is understood that claim 1 is not limited to the specific embodiment of Figs. 4A and 4B.

In Figs. 4A and 4B, the first selected stacked metal layer portion is M5 metal layer 86, and the second selected stacked metal layer portion is M6 metal layer 90. The first capacitor dielectric layer is 91, and the first capacitor metal plate layer is 92. The second capacitor dielectric layer is 93, and the second capacitor metal plate layer is 95. The second capacitor metal plate layer 95 is under the second selected stacked metal layer portion 90 and is over and spaced from the first capacitor metal plate layer 92. The metal capacitor via layer is 89, and the first via is 88.

In view of the foregoing, Applicant respectfully requests withdrawal of the rejection of claims 1-8 under 35 U.S.C. § 112, second paragraph.

Furthermore, the Abstract does describe the capacitor structure. Therefore, Applicant respectfully requests withdrawal of the objection to the Abstract.

Sections 102 and 103 Rejection

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Saia et al. (USP 5,973,908).

The Examiner alleges that Saia et al. discloses:

a first selected stacked metal layer portion 24;
a second selected stacked metal layer portion 40;
a first capacitor dielectric layer 36 over the first selected stacked metal layer portion 24;
a first capacitor metal plate layer 40 over the first capacitor dielectric layer 36 (**40 cannot be both the second selected stacked metal layer portion and the first capacitor metal plate layer**);

a second capacitor dielectric layer 44 under the second selected stacked metal layer portion 40 (**44 is disposed over, not under 40**);

a second capacitor metal plate layer 48 under the second selected stacked metal layer portion 40 and over and spaced from the first capacitor metal plate layer 40 (**48 is disposed over, not under 40**);

a metal capacitor via layer 36a between and connecting the first capacitor metal plate layer 40 and the second capacitor metal plate layer 48 (**36a is not between and connecting 40 and 48**), the metal capacitor via layer 36a forming a first terminal of the capacitor structure (**36a does not form a first terminal of the capacitor structure**); and

a first via 58 connecting the first selected stacked metal layer portion 24 and the second selected stacked metal layer portion 40 to form a second terminal of the capacitor structure (**58 does not connect 24 and 40 to form a second terminal of the capacitor structure**).

Saia et al. clearly does not disclose or suggest the elements as recited in claim 1. Thus, claim 1 is novel and patentable over Saia et al.

Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Saia et al. in view of Figs. 1A-3B of the present application. Claim 2 depends from claim 1, and is patentable over Saia et al. in view of Figs. 1A-3B, since the structure as recited in claim 1 is not taught or suggested in Saia et al. or Figs. 1A-3B.

Claims 3-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Saia et al. in view of Hoshiba (USP 5,506,748). Hoshiba is cited merely for allegedly disclosing

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that the first capacitor dielectric layer and the first capacitor metal plate layer are laterally co-extensive. Even assuming that is the case, Toshiba does not cure the deficiencies of Saia et al., in that it also fails to disclose or suggest the elements as recited in claim 1 from which claims 3-8 depend.

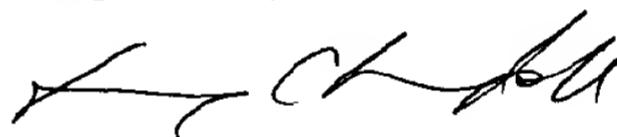
For at least the foregoing reasons, Applicant respectfully submits that claims 3-8 are patentable over Saia et al. and Toshiba.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance and an action to that end is urged.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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